Case Studies - Frontend

Fullchip SoC (RTL2GDS)

- Team : 120 (40FE, 80BE)
- Model : ODC, Turnkey
- Scope : Derivative project with reduced IPs and CPU cores than the original base design
- The design needed new RTL fabric generation, RTL Integration, Bug fixes
- Formal equivalence and Spyglass checks
- Verification of functional logic as well as DFD/DFT, including sub-system RTL updates, Verification (ATPG and GLS)
- Total of 15K Test cases
- UPF Checks and Power Aware Simulations
- Emulation for blocks and full chip using Zebu
- Re-Synthesis and Physical Design of all the partitions.
- Frequency of blocks at 1GHz
- About 10 timing corners closed
- Work involves RTL to Tape Out
- Project timelines: 15 months

SoC Fullchip DV

- Team : 18
- Model : ODC, Turnkey
- Scope : SOC - Graphics accelerator application
- Program involved developing testbench from scratch
- Team handled multiple subsystems such as DDR, Debug and peripheral subsystems
- IPs: DDR, USB, Debug, I2C, SPI, GPIO, connectivity check
- Timeline: 8 months

GPU Chipset DV

- Team : 13
- Model : T&M
- Scope : SOC Level support tasks RTL Integration, GLS, Regression/debug, Perf Sims
- Regression bucketing and generation regression reports
- SV random/Fullsim clusters
- Timeline: 8 months

PCIe G4 IP DV

- Team : 7
- Model : ODC, Milestone
- Scope : Module level and IP level DV activity using SV/UVM
- Test bench development and verification closure for multiple modules
- Integration and execution of 3rd party Verification IP suite
- Timeline : 11 months

Hard IP DV

- Team : 26
- Model : T&M
- Scope : Verification ownership of key IPs deliverables across multiple SOCs
- IP List: MIPI, Display Port, LPDDR, Mod Phy
- Supported validation of feature changes (includes verification, DFT, GLS, coverage)
- Owned IP val deliverables of SOCs (5-6 SOC/yr)
- Timeline : 11 months